AMENDMENTS TO THE CLAIMS

Claims 1-30 (Cancelled)

31. (Currently Amended) An ESD protection structure ~~formed in a semiconductor material of a first conductivity type, the semiconductor material having a dopant concentration, the structure~~ comprising:

a semiconductor region having a first conductivity type and a dopant concentration;

an isolation region ~~formed in~~ that contacts the semiconductor ~~material~~ region;

a well region of a second conductivity type ~~formed in~~ that contacts the semiconductor ~~material~~ region, the well region having a dopant concentration and not contacting a region of the second conductivity type that has a dopant concentration that is greater than the dopant concentration of the well region;

a first region of the second conductivity type ~~formed in~~ that contacts the semiconductor ~~material~~ region, the first region being spaced apart from the well region, having a dopant concentration that is greater than the dopant concentration of the well region, and being connected to a first line, no region having the second conductivity type and a dopant concentration greater than the dopant concentration of the well region lying between the first region and the isolation region; and

a second region of the first conductivity type ~~formed in~~ that contacts the well region, the second region having a dopant concentration, the first region and the second region lying on opposite sides of the isolation region, no region having the first conductivity type and a dopant concentration greater than the dopant concentration of the semiconductor ~~material~~ region lying between the second region and the isolation region, the second region being connected to a second line, the second line not being directly connected to the first line.

32. (Previously Presented) The ESD protection structure 31 wherein the well region contacts the isolation region.

33. (Previously Presented) The ESD protection structure 32 wherein the second region contacts the isolation region.

34. (Previously Presented) The ESD protection structure 33 wherein the first line includes a ground line.

35. (Previously Presented) The ESD protection structure 34 wherein the second line includes an I/O line.

36. (Previously Presented) The ESD protection structure 33 wherein the second line includes a power line.

37. (Currently Amended) The ESD protection structure of claim 33 wherein the dopant concentration of the semiconductor ~~material~~ region is less than the dopant concentration of the second region.

38. (Currently Amended) An ESD protection structure ~~formed in a semiconductor material of a first conductivity type, the semiconductor material having a dopant concentration, the structure~~ comprising:

a semiconductor region having a first conductivity type and a dopant concentration;

an isolation region ~~formed in~~ that contacts the semiconductor ~~material~~ region;

a well region of a second conductivity type ~~formed in~~ that contacts the semiconductor ~~material~~ region, the well region having a dopant concentration;

a first region of the second conductivity type ~~formed in~~ that contacts the semiconductor ~~material~~ region, the first region being spaced apart from the well region, having a dopant concentration that is greater than the dopant concentration of the well region, and being connected to a first line, no region having the second conductivity type and a dopant concentration greater than the dopant concentration of the well region lying between the first region and the isolation region; and

a second region of the first conductivity type ~~formed in~~ that contacts the well region, the second region having a dopant concentration, the first region and the second region lying on opposite sides of the isolation region, no region having the first conductivity type and a dopant concentration greater than the dopant concentration of the semiconductor ~~material~~ region lying between the second region and the isolation region, the second region being connected to a second line, the second line not being directly connected to the first line.

39. (Previously Presented) The ESD protection structure 38 wherein the well region contacts the isolation region.

40. (Previously Presented) The ESD protection structure 39 wherein the second region contacts the isolation region.

41. (Previously Presented) The ESD protection structure 40 wherein the second line includes an I/O line.

42. (Previously Presented) The ESD protection structure 41 wherein the first line includes a ground line.

43. (Previously Presented) The ESD protection structure 40 wherein the second line includes a power line.

44. (Previously Presented) The ESD protection structure 39 wherein the first line includes a ground line.

45. (Previously Presented) The ESD protection structure 44 wherein the well region does not contact a region of the second conductivity type that has a dopant concentration that is greater than the dopant concentration of the well region.

46. (Currently Amended) An ESD protection structure ~~formed in a semiconductor material of a first conductivity type, the semiconductor material having a dopant concentration, the structure~~ comprising:

a semiconductor region having a first conductivity type and a dopant concentration;

an isolation region ~~formed in~~ that contacts the semiconductor ~~material~~ region;

a well region of a second conductivity type ~~formed in~~ that contacts the semiconductor ~~material~~ region, the well region contacting the isolation region and having a dopant concentration;

a first region of the second conductivity type ~~formed in~~ that contacts the semiconductor ~~material~~ region, the first region being spaced apart from the well region, having a dopant concentration that is greater than the dopant concentration of the well region, and being connected to a first line, no region having the second conductivity type and a dopant concentration greater than the dopant concentration of the well region lying between the first region and the isolation region; and

a second region of the first conductivity type ~~formed in~~ that contacts the well region, the second region having a dopant concentration, the first region and the second region lying on opposite sides of the isolation region, no region having the first conductivity type and a dopant concentration greater than the dopant concentration of the semiconductor ~~material~~ region lying between the second region and the isolation region, the second region being connected to a second line, the second line not being directly connected to the first line.

47. (Previously Presented) The ESD protection structure 46 wherein the first line includes a ground line.

48. (Previously Presented) The ESD protection structure 47 wherein the second line includes an I/O line.

49. (Previously Presented) The ESD protection structure 46 and further comprising an amplifier having an input connected to the second region, the first region being connected to a positive differential voltage.

50. (Currently Amended) The ESD protection structure 49 and further comprising a protection diode, the protection diode having:

an insulation region ~~formed in~~ that contacts the semiconductor ~~material~~ region;

a well area of the second conductivity type ~~formed in~~ that contacts the semiconductor ~~material~~ region, the well area contacting the insulation region and having a dopant concentration;

a third region of the second conductivity type ~~formed in~~ that contacts the semiconductor ~~material~~ region, the third region being spaced apart from the well area, having a dopant concentration that is greater than the dopant concentration of the well area, and being connected to a second differential voltage, no region having the second conductivity type and a dopant concentration greater than that of the well area lying between the third region and the insulation region; and

a fourth region of the first conductivity type ~~formed in~~ that contacts the well area, the fourth region having a dopant concentration, the third region and the fourth region lying on opposite sides of the insulation region, no region having the first conductivity type and a dopant concentration greater than the dopant concentration of the semiconductor ~~material~~ region lying between the fourth region and the insulation region, the fourth region being connected to the input of the amplifier.